REMARKS

Careful consideration has been given to the Official Action of May 19, 2008, and reconsideration of the application as amended is respectfully requested.

Drawings

As required by the Examiner, submitted herewith is a new drawing illustrating the claimed invention.

Specification

To overcome the Examiner's objections to the abstract, it has been rewritten.

The specification has been amended to delete the embedded hyperlink and trademark and to cite the Maxim DS2409 reference.

The specification has also been amended to refer to the new drawing and to include reference numerals.

Claim objections and rejection

Claim 1 stands rejected under 35 USC 101 for allegedly not being a proper process claim.

Claim 1 also stands rejected under 35 USC 103(a) as being allegedly unpatentable over Applicant Admitted Prior Art (AAPA, specifically the Examiner referred to page 3, lines

1-12 which discuss the MicroLAN bus) in view of Lattice ("In-System Programming Design Guidelines for ispJTAG Devices", February 2002).

Amendments

In response, claim 1 has been canceled without prejudice, and rewritten as new claims 2, and 4-6 to be in better form without narrowing the scope. Particularly, claim 2 is directed to a system provided by the claimed invention and claims 4-6 are directed to a method of transferring discrete electrical signals using the system of claim 2.

New claim 3 recites that the first pole and the first wire are grounded to a floating ground. Support for this can be found at, for example, page 5, lines 1-4.

Discussion

The claims as now presented are clearly patentable over the cited references as will be discussed hereafter.

To reduce the noise generated by electromagnetic influence on the signal being transmitted, the claimed invention provides a system including a symmetrical two-wire communication line in which both wires are provided with a respective resistor having the same resistance, and the data is received by measuring a voltage value between the two wires. This allows a large number of devices, to be simultaneously connected to the communication line, and also allows the noise level to be reduced.

In contrast, neither AAPA nor Lattice teaches a two-wire communication line in which both wires are connected to a respective resistor having the same resistance.

Specifically, as already acknowledged by the Examiner at page 5, lines 5-7 of the Official Action, AAPA does not teach or suggest that the first wire of the communication line is grounded via an additional resistor whose value is equal to the value of the first resistor. The Examiner contends that Lattice fulfills this deficiency because it provides a pull-up resistor on the TMS signal and a pull-down resistor on the TCK signal (page 6, lines 8-13).

However, the TMS and TCK signals cannot read on the first and second wires of the claimed invention. As can be seen in the circuit diagram of the JTAG interface from the attached printout from wikipedia, the TMS (Test Mode Select) and TCK (Test Clock) signals are not used for data transfer. Only the line consisting of TDI (Test Data In) and TDO (Test Data Out) is used for data transfer. Therefore, the TMS and TCK are clearly distinguished from the two wires of the claimed invention which are used for data transfer.

Furthermore, it should be noted that the Lattice (or JTAG) technology actually represents four two-wire interfaces (each of the four ports- TDI, TDO, TCK, and TMS are coupled to the common wire (ground bus)). Since the Lattice technology is used for communication over very short distances (often within the range of the same integrated circuit board), the common wires of the four lines are often combined and shown on electrical schematic diagrams as a single wire, and sometimes not shown altogether as those of skill in the art can see the layout and understand that requirement of the common wire without

explicit indication. Therefore, each pair of these ports is not only clearly distinguished from the two wires of the claimed invention, Lattice clearly teaches away from the two wires of AAPA and one skilled in the art would not combine these references as proposed by the Examiner.

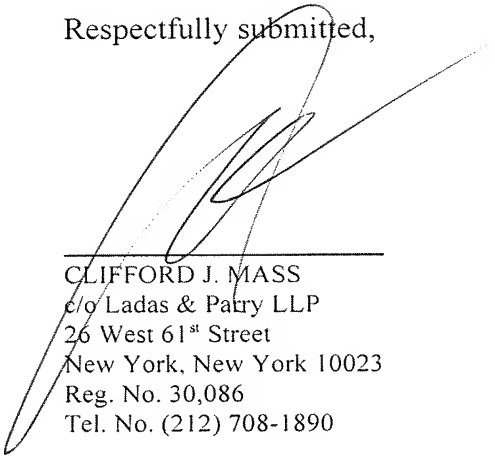
It should also be noted that AAPA and Lattice are directed to solving fundamentally different problems and one skilled in the art would respectively not combine them to "improve the noise immunity" as proposed by the Examiner. AAPA (or MicroLAN) is intended for transmission of information over long distances (hundreds of meters) and seeks to minimize the effect of electromagnetic noise from external sources (power supply lines, telephone cables, radio frequency interference, etc.). In contrast, Lattice is directed to minimizing voltage surges which may occur during power-up, which would result in the processor's error in reading voltages at the TCK and TMS inputs, which in turn, may bring about the processor's logic errors. Thus, Lattice provides pull-up and pull-down resistors to prevent voltage surges at switching on the internal power supply (noise related to the transitional processes at power-up), and has nothing to do with transmission of information or protection from electromagnetic noise.

With respect to new claim 3, it is noted that before the claimed invention, the conventional thinking was to reduce noise level by grounding the connections. In contrast, Applicant discovered that, by holding the device under a "floating" potential (or floating ground), which follows the changing voltage of noise readily and simultaneously in all the device terminals, this provides no potential difference between the terminals and thus the

noise can be minimized.

In view of the above action and comments, it is respectfully submitted that the application is in condition for allowance and early notice thereof is earnestly solicited.

Respectfully submitted,



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